IN THE SPECIFICATION:

Please replace the paragraph beginning on page 17, line 11 with the following paragraph:

According to still another exemplary aspect of the present invention, the second electrically conductive layer 165 further comprises a plurality of electrically conductive vertical interconnects 170. The vertical interconnects 170, for example, electrically connect the first electrically conductive layer 125 and the second electrically conductive layer ~~145~~ 165. A plurality of electrodes 175, for example, are further electrically connected to the second electrically conductive layer 165, therein electrically connecting the first electrically conductive layer 125 to the plurality of electrodes *via* the plurality of vertical interconnects 170. The plurality of vertical interconnects 170 may comprise, for example, a plurality of vias 180 associated with the semiconductor platform 120, wherein the plurality of vias generally extend from the top surface 127 to the bottom surface 168 of the semiconductor platform. The plurality of vias 180, therefore, electrically connect each portion 130 of the first electrically conductive layer 125 to the respective portion 167 of the second electrically conductive layer 165. Each portion 130 and 167 of the first electrically conductive layer 125 and second electrically conductive layer 165, respectively, may be electrically connected, for example, by one or more of the plurality of vias 180 (*e.g.,* portion 130A is electrically connected to portion 167A through one or more vias 180A). As Illustrated in Fig. ~~11~~ 4, for example, the plurality of vias 180 are generally oriented about the semiconductor platform 120 such that the clamping plate 110 is substantially thermally and electrically balanced.

Please replace the paragraph beginning on page 23, line 26 with the following paragraph:

Referring again to Fig. 12, act 320 describes the act of patterning a resist layer to define contact holes and gas holes. Fig. 13D illustrates the resist 416 is patterned over the backside 406 of the substrate 410, wherein the resist generally defines a contact hole ~~418~~ 420. Note that the number of contact holes ~~418~~ 420 illustrated in the figures is shown for simplicity, and numerous contact holes may be defined. The contact hole ~~418~~ 420, for example, is utilized to define a frontside contact (not shown), as will be discussed hereafter. In act 325 of Fig. 12, the contact hole is etched, wherein Fig. 13E illustrates the result, wherein the oxide layers 402 and 414 and the conductive layer 412 are etched, therein further defining the contact hole ~~418~~ 420. The resist is subsequently stripped, and in act 330 of Fig. 12, the contact hole is further etched in the substrate. Fig. 13F illustrates the result of act 330, wherein the substrate 410 is etched, and wherein the oxide layers 402 and 414 are further etched, using the conductive layer 412 as an etch stop. The oxide layers 402 and 414, can be etched using, for example, a wet etch or reactive ion etch (RIE) process.

Please replace the paragraph beginning on page 24, line 14 with the following paragraph:

Act 335 of Fig. 12 illustrates a deposition of a conductive layer over the substrate. Fig. 13G illustrates the result of act 335, wherein the conductive layer 422 is deposited over the substrate 410 (*e.g.,* a chemical vapor deposition (CVD) of 0.1 micron of WSi_2), including the frontside 404, backside 406, sidewall 408 of the substrate, as well as inside of the contact hole ~~418~~ 420. The conductive layer 422, for example, may comprise one or more of the first electrically conductive layer 125, the second electrically conductive layer 165, or the third electrically conductive layer 194, as illustrated in Figs. 2, 9, and 10.

Please replace the paragraph beginning on page 26, line 22 with the following paragraph:

The exemplary method 500 of Fig. 14 for processing the substrate begins at act 505, wherein a substrate is placed on a clamping plate having a plurality of protrusions extending from a top surface of the clamping plate. For example, the substrate 105 of Fig. 15 is placed on the plurality of protrusions (not shown) *via* a plurality of pins (*e.g.,* as illustrated in Fig. 8), wherein the plurality of pins are translated from a loading position generally above the top surface 115 of the clamping plate 110 to a processing position generally below the top surface. According to one exemplary aspect of the invention, the plurality of pins extend a minimal distance (*e.g.,* less than 1mm) from the top surface 115 of the clamping plate 110 when the pins are in the loading position. According to another exemplary aspect of the invention, the plurality of protrusions extend a first distance (not shown) from the top surface 115 of the clamping plate 110, such as a distance of approximately 1 micron, wherein the plurality of protrusions further have a surface roughness of less than approximately 100 Angstroms. Preferably, the plurality of protrusions comprise an array of micro-electromechanical structures, wherein each of the plurality of micro-electromechanical structures have a surface roughness of approximately 10 Angstroms or less.